

SN. 09/845,787

ATTORNEY DOCKET NO. FUJI:187

REMARKS

Claims 1-19 remain pending in this application for which applicants seek reconsideration.

Amendment

Claims 1, 3, 4, 6, 7, 10, and 14 and 18 have been amended to improve their form and clarity. Specifically, claims 1 and 18 have been amended to clarify that the abnormal condition -- output-- means has --at least one terminal output-- for outputting alarm signals when the abnormal condition detecting means detects the fatal abnormal condition and for outputting abnormality factor discrimination signals indicating abnormality factors contributing to the fatal abnormal condition and the precursory abnormal condition. Claim 4 has been amended to positively recite --at least one input terminal-- for inputting an abnormality factor output request signal from outside. Claim 7 has been amended to remove the use of term "themselves" by clarifying that the abnormal condition detecting means cuts off the semiconductor switching devices through the driving means. Claims 6, 10, and 14 have been placed in independent form, while adopting the above changes to claim 1 and 4 improve their form. No new matter has been introduced.

Allowable Claims

Claims 6 and 10-17 were indicated to be allowable if they are placed in independent form. In this respect, claims 6, 10, and 14 have been placed in independent form to place claims 6 and 10-17 in condition for allowance. With respect to claim 6, only part of intervening claim 4 that provides antecedent basis of the elements set forth in claim 6 has been included. Applicants submit that claim 6 is in condition for allowance.

Art Rejection

Claims 1, 7-9, 18, and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Cameron (USP 6,094,026) in view of Barritt (USP 5,648,008). Claims 18 and 19 were rejected under § 103(a) as unpatentable over these references in view of Shigekane (USP 5,115,388).

SN. 09/845,787

ATTORNEY DOCKET NO. FUJI:187

Finally, claims 2-5 were rejected under § 103(a) as unpatentable over Cameron in view of Barritt and Mano (*Computer System Architecture*). Applicants traverse these rejections because the applied references would not have taught at least the claimed abnormal condition output means as set forth in claims 1 and 18.

Claims 1 and 18 call for an abnormal condition output means having at least one output terminal for outputting alarm signals to outside when the abnormal condition detecting means detects the fatal abnormal condition and for outputting abnormality factor discrimination signals indicating abnormality factors contributing to the fatal abnormal condition and the precursory abnormal condition. Although Cameron and Barritt do include a power supply and means for protecting their devices against abnormal conditions, they do not teach an output terminal for externally outputting different signals as set forth in claims 1 and 18. In this regard, the examiner asserts that Cameron teaches an output terminal for outputting abnormality factor discriminating signals, relying on the passage set forth in column 4, lines 33-51. The output signals, however, are sent internally, one to a shutdown circuit 45 if the temperature sense circuit 40 detects certain temperature (hot) and to the frequency control 42 (to control motor speed) if the temperature sense circuit detects a different temperature (warm). Accordingly, Cameron does not teach externally outputting warning/fatal signals. Barritt teaches outputting an alarm signal to an alarm when the heating element overheats, but fails to disclose sending different alarm signals since it only detects fatal abnormal conditions.

Moreover, applicants submit that these references would not have provided the motivation for the combination suggested by the examiner because Cameron relates to a drive circuit for driving a polyphase dc motor, whereas Barritt relates to a circuit for operating a cooking apparatus and Mano relates to a serial data transfer technique. Only Shigekane discloses a power module, but does not teach outputting the alarm signals as set forth in claims 1 and 18. Specifically, Shigekane teaches outputting an alarm signal when any one of its power transistors is determined to be overheating. This is achieved by feeding the alarm signals from the power transistors to an OR circuit. Similar to Barritt, Shigekane does not output different types of alarm signals. Moreover, Shigekane OR circuit does not discriminate between different types of

SN. 09/845,787

ATTORNEY DOCKET NO. FUJI:187

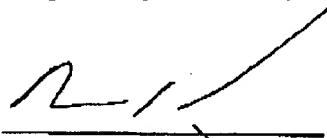
signals. Rather, it merely outputs an alarm signal when any one of the power transistors sends an alarm signal. Accordingly, applicant submits that the combination, even if it were deemed proper for argument's sake, would not have taught the claimed invention.

The other secondary reference, Mano, would not have alleviated the shortcomings of the other references.

Conclusion

Applicants submit that claims 1-19 patentably distinguish over the applied references and in condition for allowance. Should the examiner have any issues concerning this reply or any other outstanding issues remaining in this application, applicants urge the examiner to contact the undersigned to expedite prosecution.

Respectfully submitted,

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